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# NEXT GENERATION CLASS Y: FINE PITCH FLIP CHIP ON ORGANIC PACKAGE TECHNOLOGY

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Colorado Springs

2017 NEPP Electronics Technology Workshop

# Cobham-NEPP Collaboration History

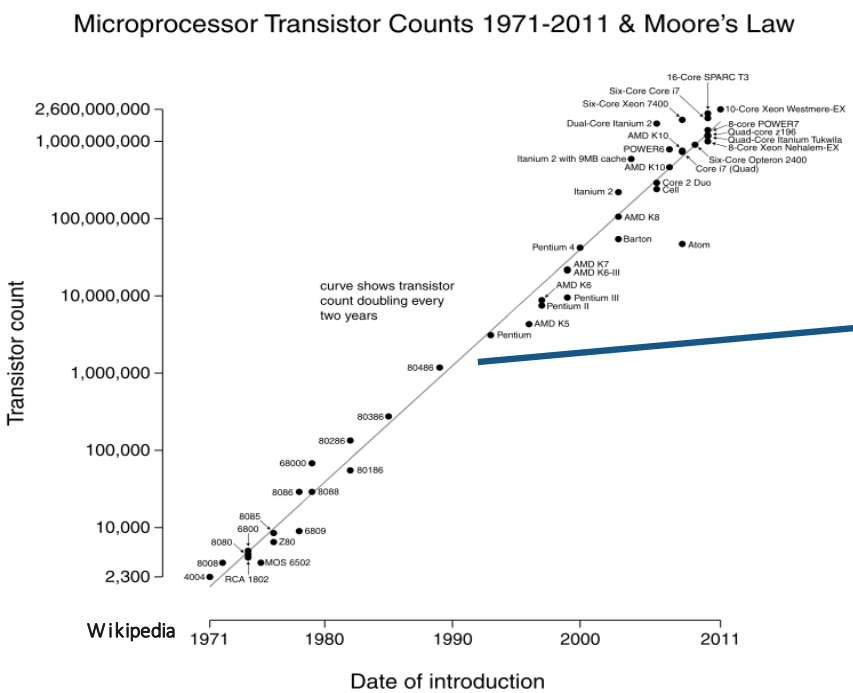
## Projects and Acknowledgements

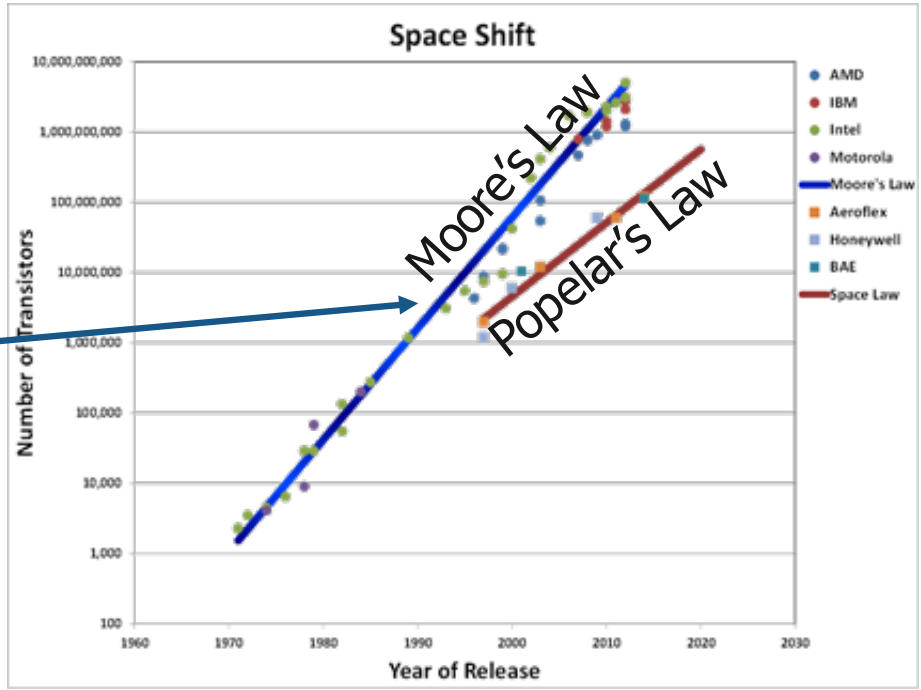
- Cobham-NEPP collaboration projects
  - *Aeroflex Technology as Class-Y Demonstrator*
    - Completed October 2014
  - *Flip Chip on Organic Feasibility Study*
    - Completed March 2017
  - *Fine Pitch Flip Chip on Organic Development*
    - Commenced March 2017
- Acknowledgements
  - *Jong-ook Suh, Ph.D., JPL Materials Scientist and Engineer*
    - Provided invaluable guidance in scoping and executing these studies
  - *Rich Measmer, Cobham Package and Process Development Engineer*
    - Critical test vehicle procurement and assembly process development
  - *Funding provided by NASA NEPP program*
    - NEPP funding is gratefully acknowledged, without which these studies would not have been possible

# Cobham Class Y Flip Chip Technology

## Popelar's Law – Moore's Law Adjusted for Space Applications (a.k.a. Space Law)

- Moore's Law: The number of transistors will double every two years
- Popelar's Law: The number of transistors will quadruple every six years
- *Popelar lags Moore, and the gap is only growing*




***Flip chip technology is critical for closing the gap between Popelar and Moore***

# Cobham Class Y Flip Chip Technology

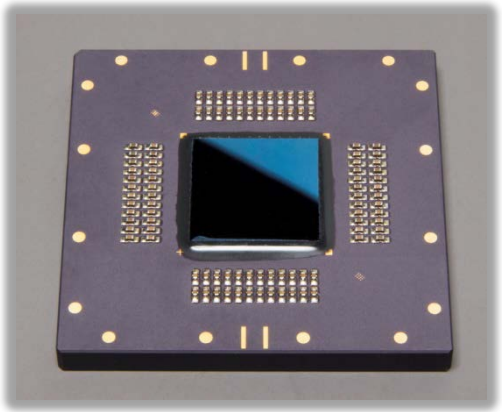
## Class Y Technology Definition

- MIL-PRF-38535 Revision K – released on December 2013
  - *Defines for the first time Class Y requirements for ceramic non-hermetic packages for space applications*
    - *Implies flip chip on ceramic assembly technology*
    - Accommodates de-coupling capacitor attach and heat sink attach
  - First DLA Class Y flip chip audit completed at Cobham Semiconductor Solutions COS facility in August 2014
    - *First DLA Class Y certification awarded to the Cobham COS facility in December 2014*
  - Stipulates that a Package Integrity Demonstration Test Plan (PIDTP) be performed for all new package technologies
    - Flip chip assembly, Chip cap attach, Heat sink attach all require PIDTP reliability assessments
    - *PIDTP reliability assessments completed by Cobham in December 2015 in support of its UT1752FC Class Y package qualification effort*

# Cobham Class Y Flip Chip Technology

## Class Y Technology as a 90nm Enabler

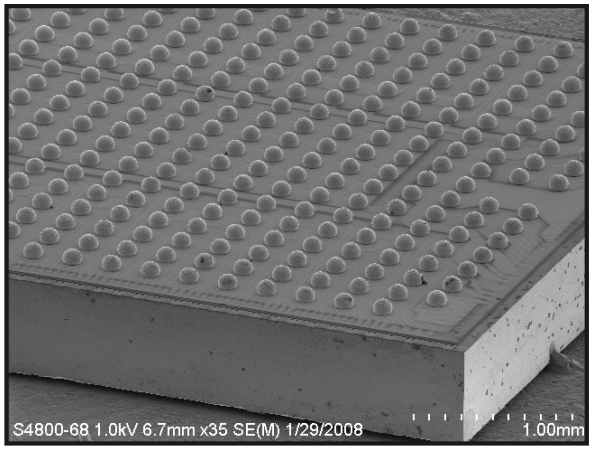
- ***UT1752FC Class Y Non-hermetic Package Technology for Space***
  - Flip chip on ceramic, with decoupling capacitors and heat sink attach
  - 1752 pin ceramic LGA/CGA on a 1.00mm pitch; optional solder column attach
- ***90nm ASIC Class Y Assembly***
  - 90nm SerDes technology, enabled by Class Y package technology
  - Product qualification scheduled to complete in 2017

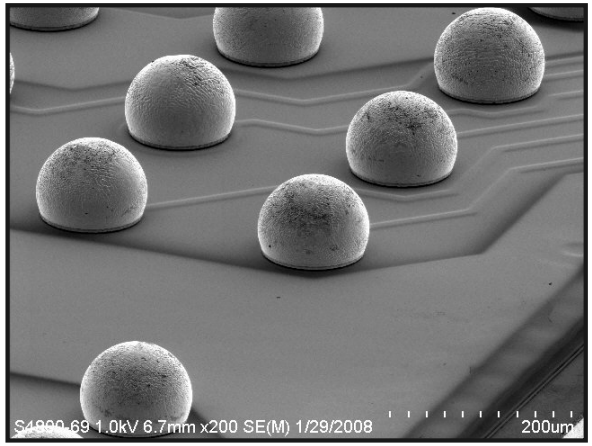


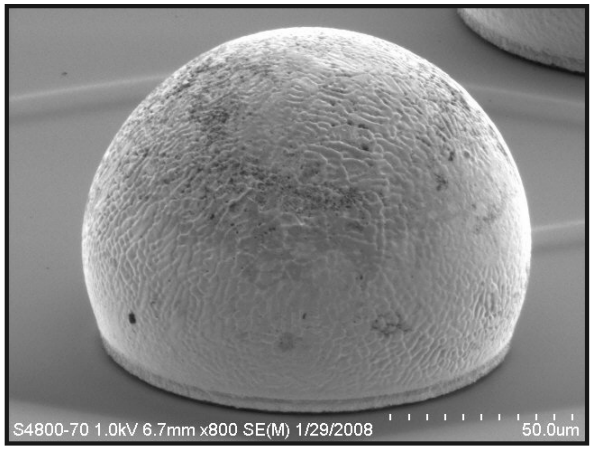

# Cobham Class Y Flip Chip Technology

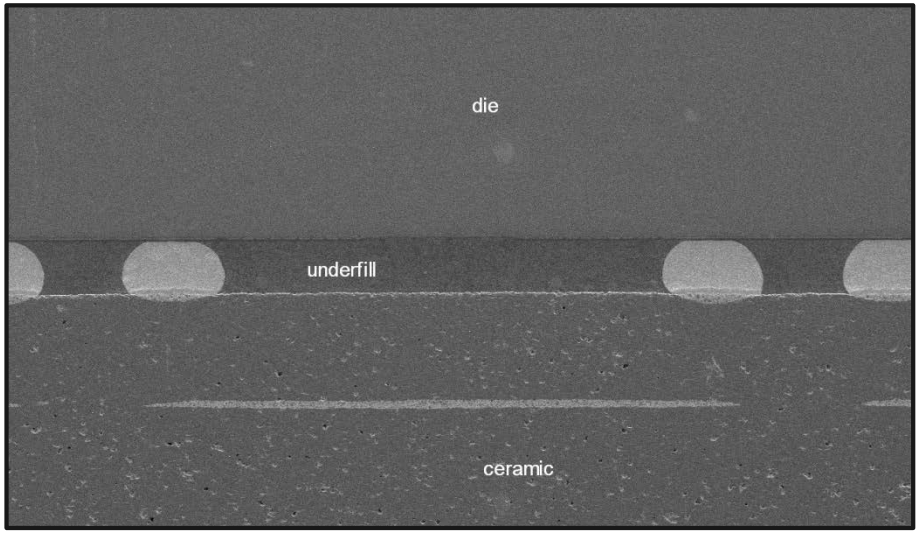
## Flip Chip Assembly

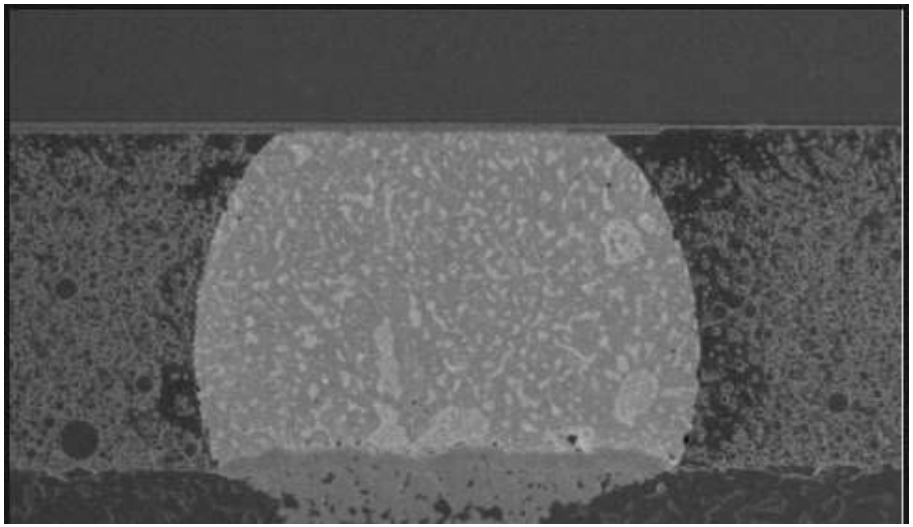
- ***Solder bump flip chip interconnects – wafer bumping through assembly***



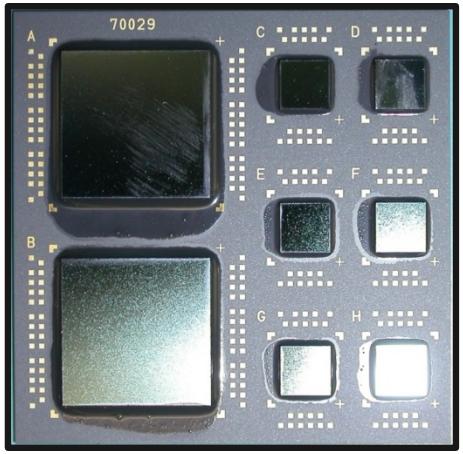



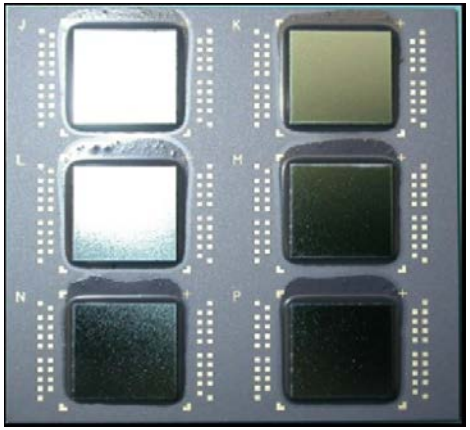



# Cobham Class Y Flip Chip Technology

## Class Y Flip Chip PIDTP

- *Flip Chip on Ceramic Daisy Chain Test Vehicles*



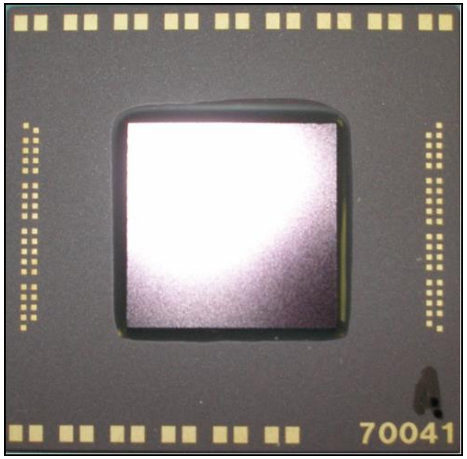

5x5mm

10x10mm

15x15mm

20x20mm

25x25mm




# Cobham Class Y Flip Chip Technology

## Class Y Flip Chip PIDTP

- ***Flip Chip PIDTP Results***

| Test Type | Test Method | Criteria | Status |
|---|---|---|---|
| Wafer Level Acceptance | Bump Yield<br>• Automated optical inspection | Bump defect rate < 200 ppm | Pass |
| Wafer Level Acceptance | Bump Height<br>• Automated optical inspection | Nominal +/- 15 µm | Pass |
| Wafer Level Acceptance | Bump Shear<br>• JESD22-B117A | Minimum load of 3 mg/µm$^2$ | Pass |
| Die Shear Assembly Monitor | TM 2011, Condition F<br>• Pre underfill | Minimum load of 5 gr/bump | Pass |
| X-Ray Assembly Monitor | TM 2012<br>• Post underfill | Solder joint voids < 25% of bump diameter | Pass |
| CSAM Assembly Monitor | TM 2030<br>• Post underfill | Underfill void content < 10% of die area | Pass |
| Cross Section Assembly Monitor | IAW Aeroflex specification 49210<br>• Post underfill | 0 defects allowed related to solder joints or underfill | Pass |

# Cobham Class Y Flip Chip Technology

## Class Y Flip Chip PIDTP

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- ***Flip Chip PIDTP Results (continued)***

| Test Type | Test Method | Criteria | Status |
|---|---|---|---|
| Temperature Cycle | TM 1010, Condition B<br>• 250 cycle endpoints, or as appropriate<br>• Test to failure, or 3000 cycles, whichever occurs first | Continuity endpoint testing; >15% increase in daisy chain resistance constitutes failure | Pass |
| 125°C High Temperature Storage<br><br>150°C High Temperature Storage | JESD22-A103C<br>• High temperature storage at 125°C and 150°C<br>• Endpoints at 0, 250, 500, 750, 1000, 1500 and 2000 hours<br>TM 2011, Condition F<br>• Die shear at each endpoint<br>• 6 die per endpoint; no underfill | Minimum load of 5 gr/bump | Pass |
| Multiple Reflow | JESD22-A113-B<br>• Multiple reflows; eutectic profile<br>• Endpoints at 0, 1, 5, 10, 15 and 20 reflows<br>TM 2011, Condition F<br>• Die shear at each endpoint<br>• 6 die per endpoint; no underfill | Minimum load of 5 gr/bump | Pass |

# Class Y Demonstrator

## Cobham-NEPP Collaboration

- *Collaborative effort between Cobham (Aeroflex) and NEPP/JPL to study the reliability of Cobham technology as a Class Y demonstrator*
  - NEPP/JPL Report: *Aeroflex Technology as Class-Y Demonstrator*
  - JPL Publication 14-16 9/14 (October 2014)
    - Authors: Jong-ook Suh, Scott Popelar
- *Electromigration of flip chip solder joint interconnect*
  - Electromigration characterization study
  - Effect of current stressing on flip chip solder interconnect strength
- *Synergistic effect of pre-conditioning on temperature cycle testing*
  - Moisture loading, Multiple reflows, Vacuum aging, Current stressing
- *Effect of ramp rate on temperature cycle testing*
  - 3.5°C/min fast ramp rate versus 0.2°C/min slow ramp rate

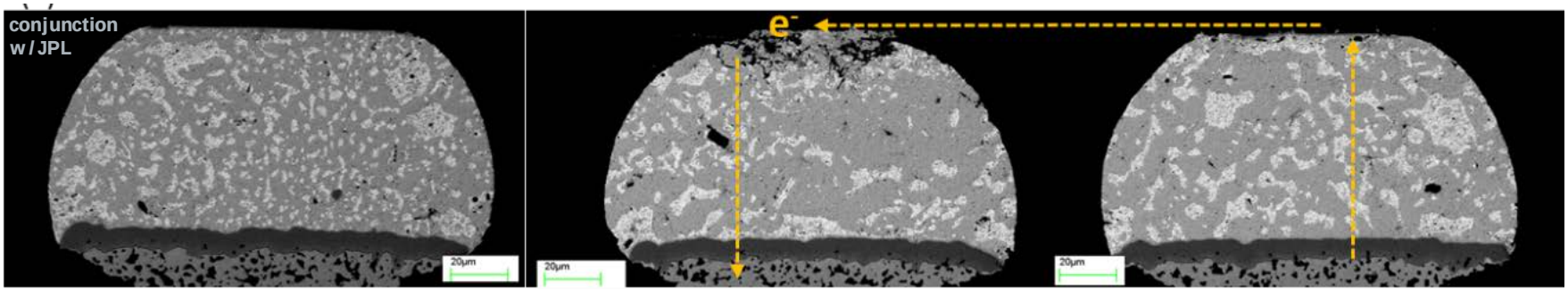
# Class Y Demonstrator

## Cobham-NEPP Collaboration

- Black's Equation

$$MTTF = Aj^{-n} \exp \frac{E_a}{kT}$$

- Accelerated current stressing conditions
  - 1A passed through 639 daisy chained interconnects (j = $2.0 \times 10^4$ A/cm$^2$)
  - Joule heating to 115°C
  - *Time to failure estimated at 5-8 days*
  - *Predicted time to failure 7.5-12.4 days*
- Use conditions (example)
  - 30mA current at 80°C junction temperature
  - *Predicted time to failure 168 years*



# Class Y Demonstrator

## Cobham-NEPP Collaboration

- *TM1010 Condition B Temperature Cycle Results (-55/125°C)*
  - 15x15mm daisy chain die size
  - Comparison of fast ramp rate results below
  - *No slow ramp failures after 3000 cycles*

| Precondition | Weibull Life | Weibull Slope | Weibull Fit $R^2$ |
|---|---|---|---|
| Baseline (no precondition) | 3629 | 6.3 | 0.9613 |
| Moisture Loading (27 days at 85°C/85%) | 2438 | 7.5 | 0.9717 |
| Multiple Reflow (5x eutectic reflows) | 5237 | 6.4 | 0.9348 |
| Vacuum Aging (3 months in $10^{-7}$ Torr at 135°C) | 5474 | 8.9 | 0.9402 |
| Current Stressing (96 hours at 1A and 115°C) | 3978 | 4.9 | 0.8013 |

# Next Generation Class Y Technology

## Limitations of Flip Chip on Ceramic

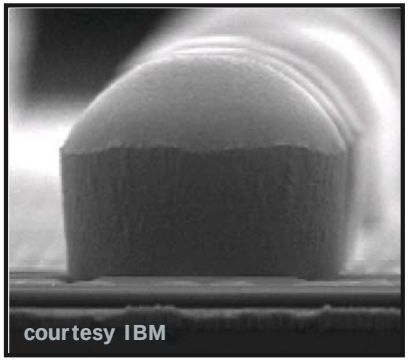
- ***Ceramic package technology limitations***
  - Dielectric constant of alumina (9.8) limits performance/speeds to ~6Gbps
  - Routing is limited to 50µm lines and spaces
  - CTE mismatch between ceramic package (~6ppm/C) and board (~17ppm/C) becomes significant for large I/O package footprints
  - Cost for ceramic packages increases exponentially with large I/O footprints
- ***Solder bump flip chip pitch limitations***
  - Solder interconnects are nominally limited to pitches of 200µm if the goal is to maintain a bump height of 100µm
  - Below 200µm pitches, the solder bump will have to shrink (~1/2 pitch), resulting in a corresponding decrease in reliability
  - Sub-90nm technology nodes typically utilize fine pitch die I/O (150µm or less)

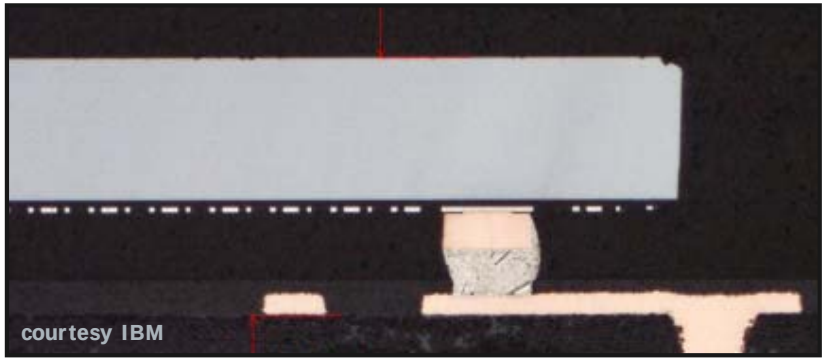
***Next Generation Class Y Technology required to enable sub-90nm technology***

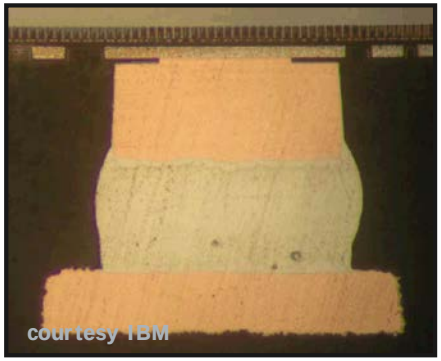
# Next Generation Class Y Technology

## Flip Chip on Organic Technology as a sub-90nm Enabler

- ***Kyocera High Density Build-Up (HDBU) organic substrate technology***
  - Capable of handling speeds typical of sub-90nm technology nodes (>10Gbps)
  - Capable of routing with 12µm lines and spaces
  - Lower CTE mismatch between organic package (~11ppm/C) and board (~17ppm/C)
  - Lower cost solution for large I/O package footprints
- ***Copper pillar flip chip interconnects***
  - Capable of handling fine pitches typical of sub-90nm technology nodes (100-150µm)
  - Greater electromigration resistance compared to solder bump interconnects




***Space Law requires qualification of Next Generation Class Y Technology***

# Flip Chip on Organic Feasibility Study

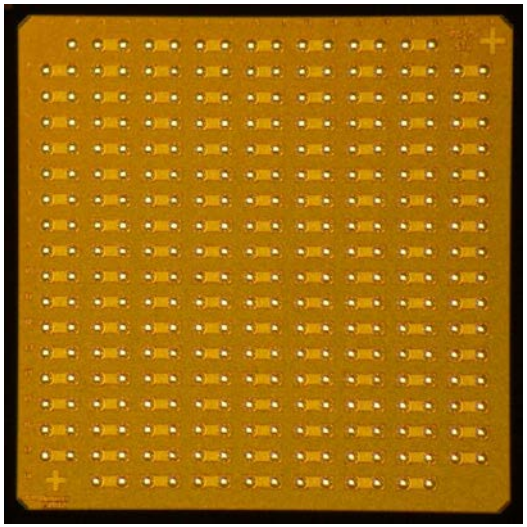
## Cobham-NEPP Collaboration

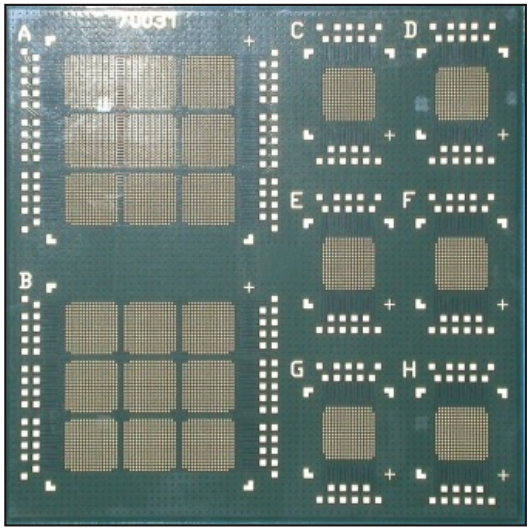
- *Collaborative effort between Cobham and NEPP/JPL to study the feasibility of flip chip on organic technology for space applications*
  - Technical leads: Scott Popelar, Jong-ook Suh, Rich Measmer
  - Duration: December 2016 thru March 2017
  - Report: 2017 GOMACTech Conference
- *Identify and vet different underfill materials as to their compatibility and reliability with respect to flip chip on organic assembly*
  - Outgassing, Mechanical characterization
- *Establish a reliability baseline for flip chip assembly to organic substrates using existing test vehicles*
  - Stud pull and CSAM assembly monitors
  - High temperature storage, Temperature cycling, Moisture loading effect

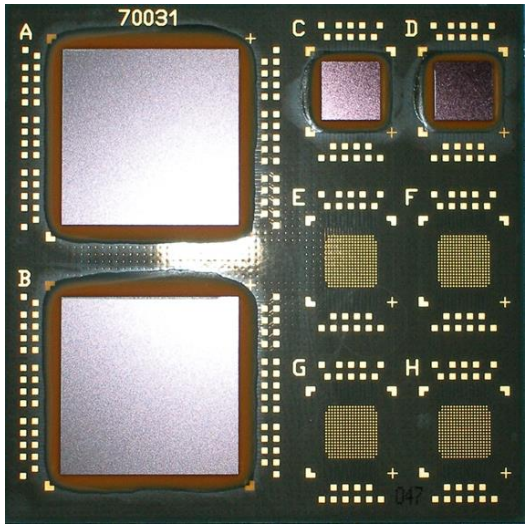
# Flip Chip on Organic Feasibility Study

## Test Vehicle Description

- ***FA10 Flip Chip Daisy Chain Test Die***
  - 254µm bump pitch, 110µm bump height
  - Eutectic Sn/Pb solder alloy; FCI wafer bumping technology
  - 5x5mm (317 I/O) and 15x15mm (2,853 I/O) die sizes
- ***Organic High Density Build-Up (HDBU) test substrate***
  - Dual-sided, 1.0mm thick
  - 127µm solder mask defined pads with ENIG plating



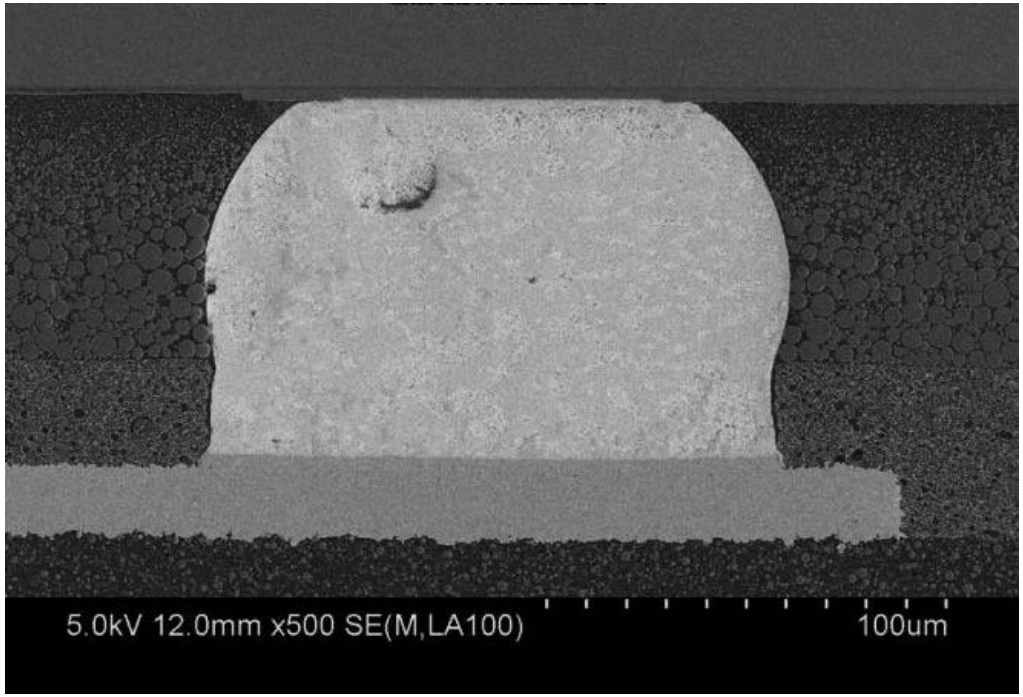


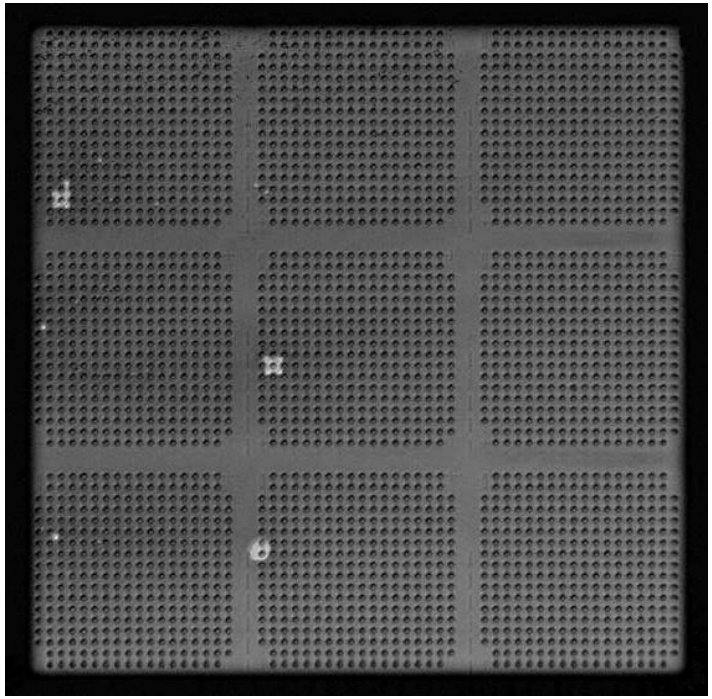



# Flip Chip on Organic Feasibility Study

## Assembly Monitors

- ***Cross-section and CSAM Assembly Monitors***
  - Solder joint integrity at die and substrate interface
  - Minimal underfill void content (much less than 10% allowable)



# Flip Chip on Organic Feasibility Study

## Underfill Characterization

- ***Underfill Material Properties***
  - "Control" qualified for Class Y applications; meets TM5011 requirements
    - Tg = 120°C, CTE = 28ppm/C
  - Underfill "A" selected due to its Tg that is higher than that of the Control
    - Tg = 135°C, CTE = 27ppm/C
  - Underfill "B" selected due to its CTE being lower than that of the Control
    - Tg = 115°C, CTE = 22ppm/C
  - ***All three underfill materials meet outgassing requirements***

| Underfill | IWV per TM1018 (5000ppm limit) | TML per ASTM E-595 (1.0% limit) | CVCM per ASTM E-595 (0.1% limit) |
|---|---|---|---|
| Control | 816ppm | 0.24% | 0.01% |
| A | 518ppm | 0.18% | 0.00% |
| B | 612ppm | 0.19% | 0.01% |

# Flip Chip on Organic Feasibility Study

## Reliability Baseline

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- ***Reliability Assessments***

| Test Type | Test Method | Criteria | Status |
|---|---|---|---|
| Flip Chip Pull-Off Test<br>Assembly Monitor | MIL-STD-883, TM 2031<br>• Pre underfill | Minimum load of 18.1kg | Pass |
| CSAM<br>Assembly Monitor | MIL-STD-883, TM 2030<br>• Post underfill | Underfill void content < 10% of die area | Pass |
| Stud Pull Test<br>Assembly Monitor | MIL-STD-883, TM 2027<br>• Post underfill | Minimum load of 10.7kg | Pass |
| Cross Section<br>Assembly Monitor | IAW Cobham specification 49210<br>• Post underfill | 0 defects allowed related to solder joints or underfill | Pass |
| High Temperature Storage Testing | JEDEC JESD22-A103C<br>• High temperature storage at 125°C and 150°C<br>• Endpoints every 250 hours, up to 2000 hours; extended testing to 4000 hours | Continuity endpoint testing; >15% increase in daisy chain resistance constitutes failure | Pass 4000 hrs at 125°C |

# Flip Chip on Organic Feasibility Study

## Reliability Baseline

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- *Reliability Assessments (continued)*

| Test Type | Test Method | Criteria | Status |
|---|---|---|---|
| Temperature Cycle Testing<br>Fast Ramp Rate (~3.5C/sec)<br>Slow Ramp Rate (~0.2C/sec) | MIL-STD-883, TM 1010, Condition B (-55/125°)<br>• 250 cycle endpoints, or as appropriate<br>• Test to failure, or 3000 cycles, whichever occurs first<br>• Failure analysis | Continuity endpoint testing; >15% increase in daisy chain resistance constitutes failure | Refer to following slides |
| Moisture Loading | JEDEC JESD22-A101<br>• 1000 hours at 85°C/85%RH<br>• Endpoint testing at 0 and 1000 hours<br>• Continuity testing<br>• Stud pull testing per TM 2027 | Continuity endpoint testing; >15% increase in daisy chain resistance constitutes failure | Pass |
| Moisture Loading<br>Temperature Cycle Testing | JEDEC JESD22-A101<br>• 1000 hours at 85°C/85%RH<br>MIL-STD-883, TM 1010, Condition B (-55/125°C)<br>• 250 cycle endpoints<br>• Test to 3000 cycles | Continuity endpoint testing; >15% increase in daisy chain resistance constitutes failure | Refer to following slides |

# Flip Chip on Organic Feasibility Study

## High Temperature Storage

- ***125°C High Temperature Storage Testing***
  - 4000 hours completed with no failures detected
- ***150°C High Temperature Storage Testing***
  - First failure detected at 750 hour endpoint
  - Failures indicative of UBM consumption due to thermal migration
- ***No HTS dependence on underfill material observed***
  - All three underfill materials pass 4000 hours at 125°C
  - Failures at 750 hours at 150°C with all three underfill materials
- ***No HTS dependence on substrate material observed***
  - Flip chip on organic results consistent with flip chip on ceramic results
  - No failures at 125°C after 4000 hours
  - HTS at 150°C limited by UBM consumption

# Flip Chip on Organic Feasibility Study

## Temperature Cycle Testing

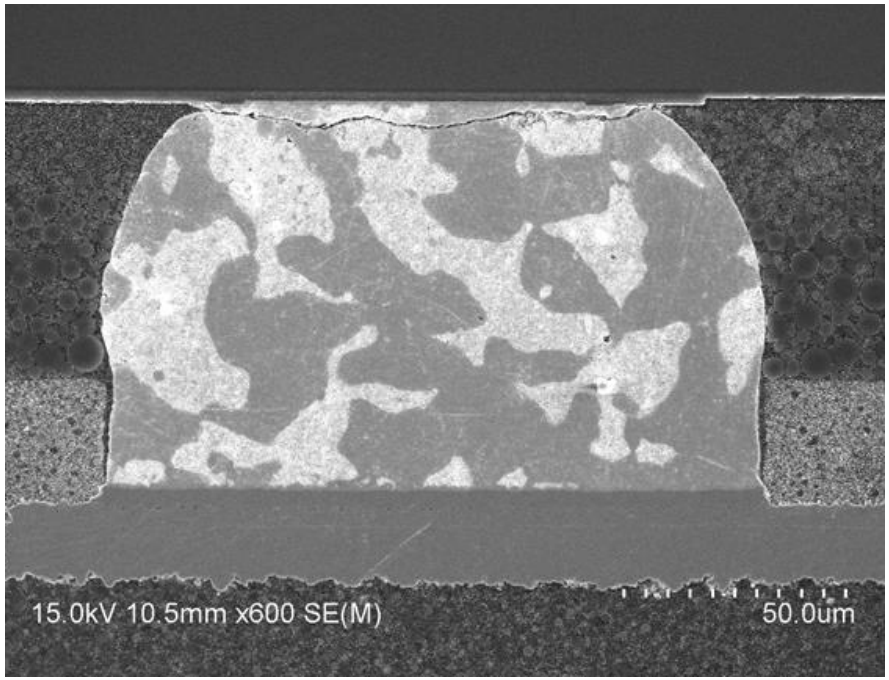
- ***Fast Ramp Rate Condition B Temperature Cycle Testing (-55/125°C)***
  - 3000 fast ramp rate cycles completed (~3.5°C/sec)
- ***Die Size Dependence Observed (5x5mm vs 15x15mm die size)***
  - No failures with 5x5mm die, across all underfill materials
- ***Underfill Dependence Observed (15x15mm die size)***
  - Control: First failure at 250 cycle endpoint; 70% failure at 3000 cycles
  - A: First failure at 2000 cycle endpoint; 30% failure at 3000 cycles
  - B: First failure at 2250 cycle endpoint; 10% failure at 3000 cycles
- ***Slow Ramp Rate Condition B Temperature Cycle Testing (-55/125°C)***
  - 3000 slow ramp rate cycles completed (~0.2°C/sec)
  - Similar failure rates compared to fast ramp rate temperature cycle testing

***Underfill B exhibits superior resistance to temperature cycling***

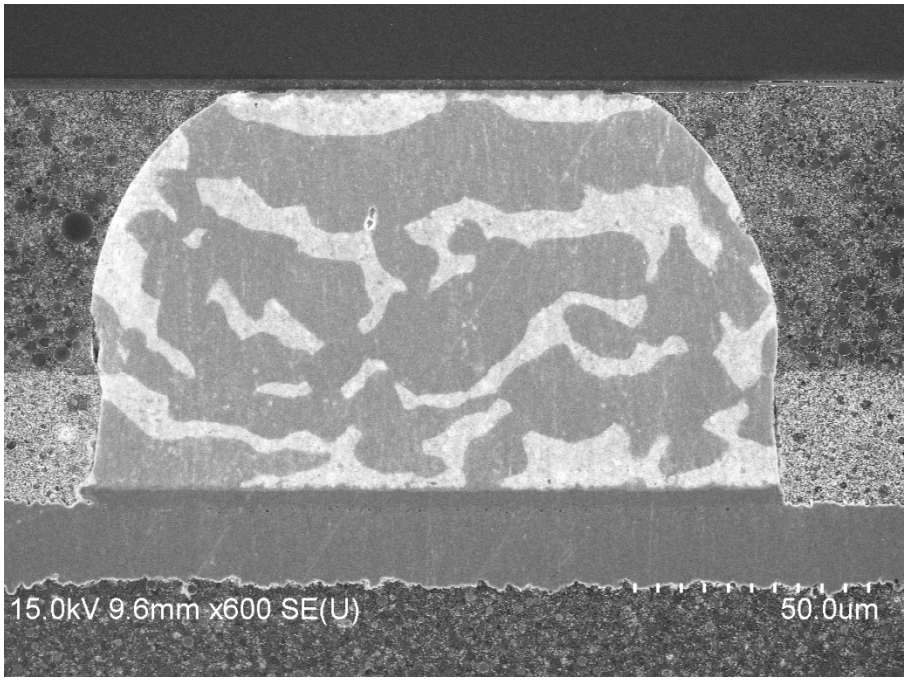
# Flip Chip on Organic Feasibility Study

## Temperature Cycle Testing

- ***Fast Ramp Rate Temperature Cycle Cross Section Failure Analysis***
  - Significant grain coarsening between lead and tin components (typical)
  - Interconnect failure due to underfill delamination (Underfill A)




Failed solder interconnect after 3000 cycles (Underfill A)

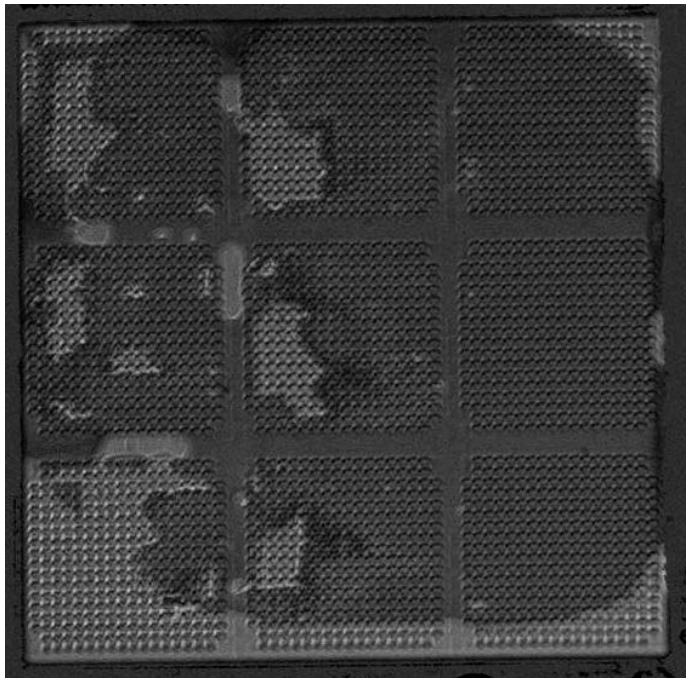



Passing solder interconnect after 3000 cycles (Underfill B)

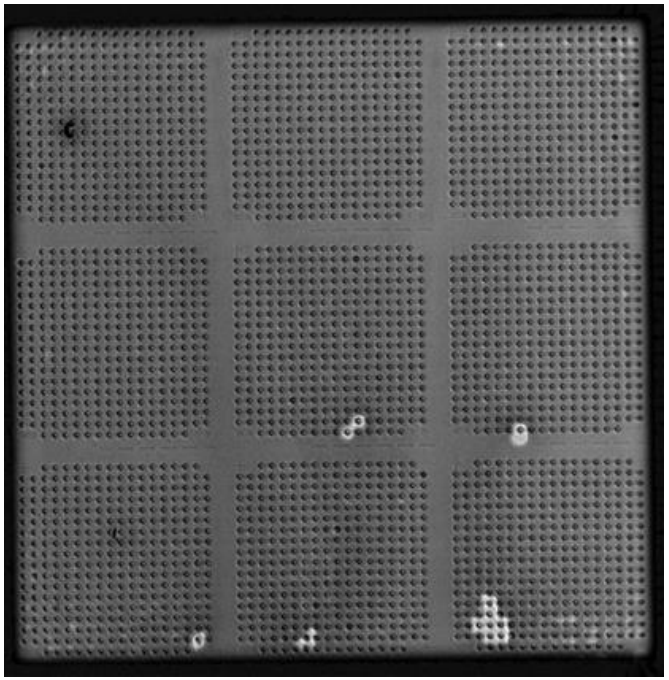
# Flip Chip on Organic Feasibility Study

## Temperature Cycle Testing

- ***Fast Ramp Rate Temperature Cycle CSAM Failure Analysis***
  - CSAM analysis performed after 3000 cycle endpoint
  - Evidence of delamination with Underfill A
  - No evidence of underfill delamination with Underfill B



Sample with underfill delamination



Sample without underfill delamination

# Flip Chip on Organic Feasibility Study

## Moisture Loading Effect

- ***Moisture Loading***
  - 1000 hours completed at 85°C/85%RH moisture loading
  - All parts pass continuity testing and stud pull monitor
- ***Effect on Fast Ramp Rate Temperature Cycle Testing (3000 cycles)***
  - Accelerated failure rate with Control and Underfill A
  - No effect on failure rate observed with Underfill B
- ***Effect on Slow Ramp Rate Temperature Cycle Testing (3000 cycles)***
  - Control underfill exhibited improvement with moisture loading
  - Accelerated failure rate with Underfill A
  - No effect on failure rate observed with Underfill B

***Underfill B exhibits superior resistance to moisture loading effects***

# Flip Chip on Organic Feasibility Study

## Class Y and Organic Flip Chip Comparison

- *Condition B Temperature Cycle Results after 3000 cycles (% failures)*

| 3000 Temperature Cycle Endpoint<br>15x15mm Daisy Chain Die Size | | | | | |
|---|---|---|---|---|---|
| | | w/o Moisture Loading | | w/ Moisture Loading | |
| Ramp Rate | Underfill | Class Y | Organic | Class Y | Organic |
| Fast | Control | 40% | 70% | 100% | 100%<br>(250TC) |
| | A | n/a | 30% | n/a | 100%<br>(500TC) |
| | B | n/a | 10% | n/a | 10% |
| Slow | Control | 0% | 100% | 0% | 10% |
| | A | n/a | 80% | n/a | 100%<br>(1000TC) |
| | B | n/a | 10% | n/a | 10% |

# Flip Chip on Organic Feasibility Study

## Cobham-NEPP Collaboration

- Conclusions
  - *The study demonstrates the feasibility of flip chip on organic substrate technology for use in space applications*
    - Underfill B flip chip on organic assemblies exhibit comparable reliability to Class Y flip chip on ceramic assemblies with the Control underfill
  - Underfill selection with respect to temperature cycle resistance and influence of moisture loading is critical
    - Underfill B clearly outperforms Control and Underfill A materials
    - Underfill B has better compatibility with respect to adhesion and CTE mismatch
- Next Steps
  - Perform reliability assessment utilizing fine pitch daisy chain test vehicle
  - *Evaluate copper pillar flip chip interconnects*

***Kick off Fine Pitch Flip Chip on Organic Development project***

# Fine Pitch Flip Chip on Organic Development

## Cobham-NEPP Collaboration

- ***Collaboration between Cobham and NEPP/JPL to evaluate the reliability of fine pitch flip chip on organic technology for space applications***
  - Technical leads: Scott Popelar, Jong-ook Suh, Rich Measmer
  - Duration: March 2017 thru June 2018
- ***Test Vehicle Design and Procurement***
  - Procure fine pitch (150µm) daisy chain test vehicle from Practical Components
  - Design and procure daisy chain HDBU organic test substrate from Kyocera
  - Evaluate supply chain for eutectic Sn/Pb copper pillar wafer bumping
- ***Copper Pillar Assembly Development***
  - Vet flux and underfill material options for copper pillar assembly
  - Develop copper pillar flip chip assembly processes
  - Optimize underfill process with respect to voiding, etc.
- ***Reliability Assessments***
  - Test vehicle assembly and assembly monitors
  - Assess fine pitch copper pillar flip chip on organic reliability
    - High Temp Storage, Moisture Loading, Temperature Cycle Testing

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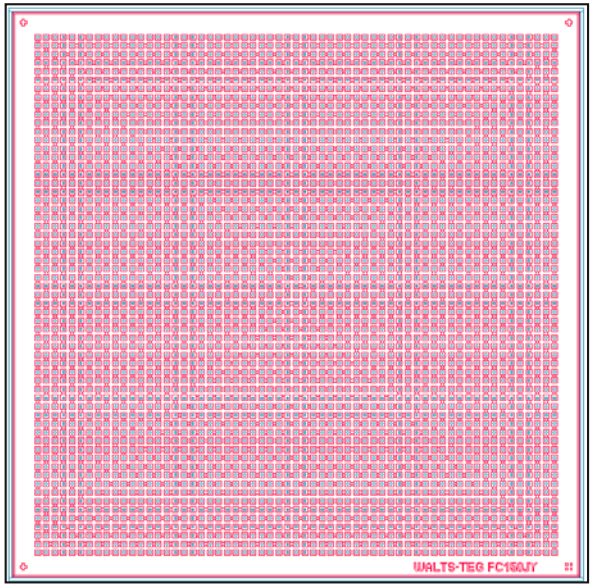
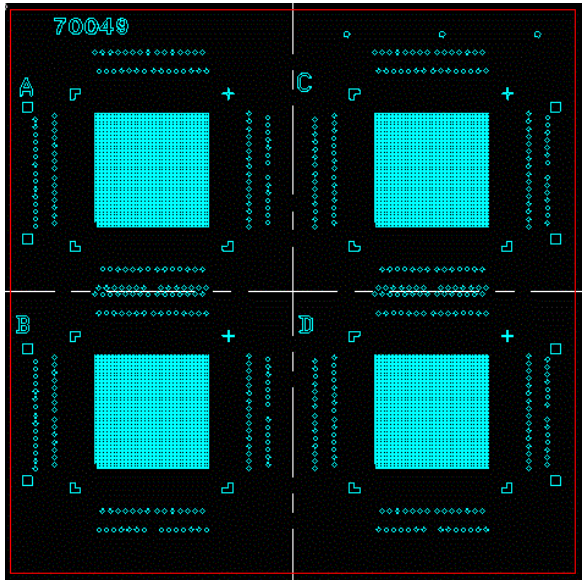
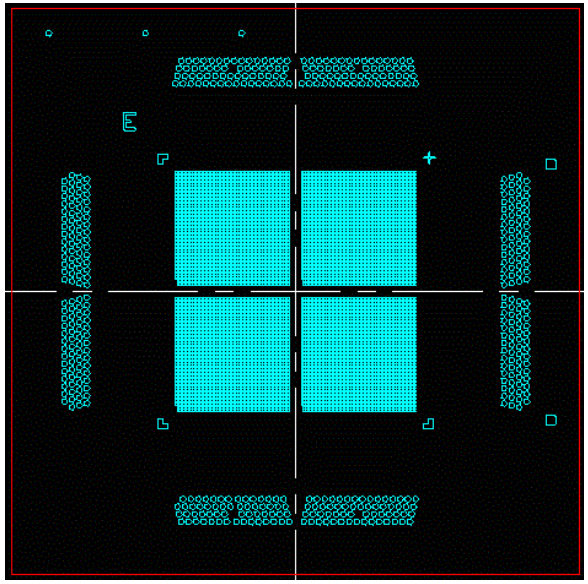
- ***WC-150 Flip Chip Daisy Chain Test Die***
  - 150µm bump pitch; 40µm copper pillar bump, 25µm eutectic Sn/Pb solder cap
  - 10x10mm (3,718 I/O) and 20x20mm (14,872 I/O) die sizes
- ***Organic High Density Build-Up (HDBU) test substrate***
  - Dual-sided, 1.0mm thick
  - 80µm solder mask defined pads with ENIG plating and eutectic SOP



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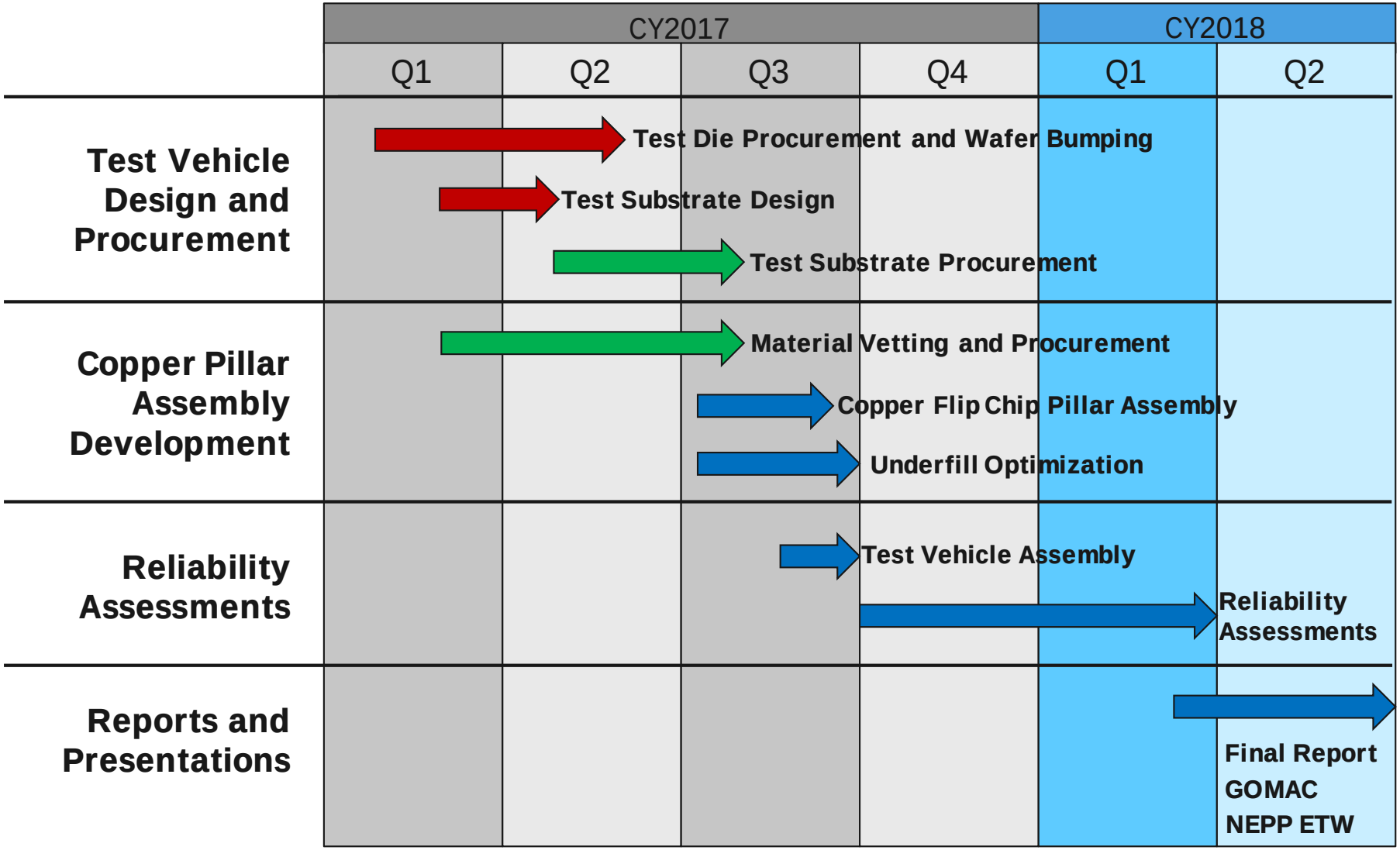

# Next Generation Class Y Technology

## Where are we going?

- Next Generation Class Y Technology
  - *Copper pillar flip chip on organic*
  - BGA second level interconnects instead of CGA
  - Use of BME decoupling capacitors?
  - New heat sink technologies?
  - Precursor to 2.5D/3D package technology qualification
- MIL-PRF-38535 Class Y
  - *Class Y currently does not accommodate organic substrates*
  - Should Class Y definition be amended/extended to capture Next Generation Class Y technology, or should a new designation be created?
- JEDEC Task Group
  - *When does it makes sense to create a dedicated task group chartered with evaluating Next Generation Class Y package technology?*
    - Is it too early? Is it too late?
  - Discuss further during September JEDEC meetings

***Next Generation Class Y Technology… to be continued***